9 A Silicon Detector for the DØ Experiment at the Tevatron

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in collaboration with:
the DØ Run IIb silicon detector group: CINVESTAS, Mexico City, Mexico, Fermi National Accelerator Laboratory, Batavia, USA; Kansas State University, Manhattan, USA; Moscow State University, Russia; State University of New York at Stony Brook, New York, USA; University of Illinois, Chicago, USA; University of Washington, Seattle, USA.

The full DØ collaboration consists of 79 institutes from the countries Argentina, Brazil, China, Czech Republic, Colombia, Ecuador, France, Germany, India, Korea, Mexico, Netherlands, Poland, Russia, Sweden, United Kingdom, United States of America and Vietnam.

(DØ Collaboration)

The Run IIa phase of the Tevatron $p\bar{p}$ collider at Fermilab, USA, has started in 2001. It offers an outstanding research programme [1] in high energy physics over the next three years for both of the experiments CDF and DØ which are operational at the Tevatron. Because of the tantalising physics prospects a higher integrated luminosity will bring, Fermilab extends the running of the Tevatron collider, called Run IIb, which could deliver a total integrated luminosity of 15 fb^{-1} in the years 2004-2007. To optimise its physics capability for the future run, the existing silicon detector of the DØ experiment is being replaced [2]. This replacement is even necessary, since the present silicon vertex detector would not survive the harsh radiation environment of Run IIb [3]. The new silicon device will be the centrepiece detector to perform the rich physics programme, which is highlighted by a significant chance of a Higgs boson discovery, if its mass is below 115 GeV [4].

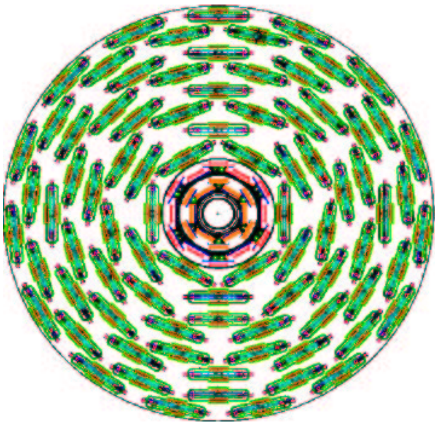

Figure 9.1: *End view of the DØ 6-layer silicon device.*

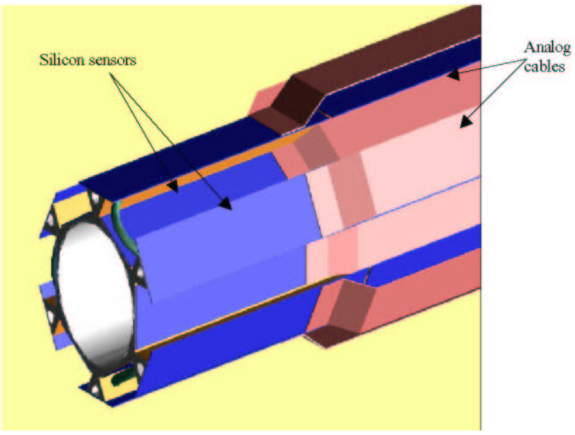

Figure 9.2: *The innermost silicon layer close to the beam pipe. The analog cable routing the silicon signals to the hybrid is also shown.*

The main requirements for the silicon detector are efficient and reliable tracking, precise vertex measurements and radiation hardness in a very harsh charged hadron radiation environment of up to 15 MRad. All of these goals will be met with the designed 6-layer single sided silicon device segmented in two barrels around the beam pipe and covering a pseudorapidity range of $|\eta| \leq 2.5$. Fig. 9.1 shows an axial view of the Run IIb silicon tracker. The track lever arm of the detector between the innermost silicon layer and the outermost one will be 150 mm. The outer layers are constructed of 60 μm readout pitch silicon and provide hits essential for improved pattern recognition in a high occupancy environment. In addition, two inner layers 0/1, constructed with 50/58 μm readout pitch silicon sensors with intermediate strips at 25/29 μm, provide precise coordinate measurements essential for good secondary vertex separation and excellent impact parameter resolution in the $r-\varphi$ plane.

Based on this design a total of 2200 single sided silicon sensors in 6”-wafer technology will be used, giving more than 950,000 readout channels. The prototyping, testing and assembly of the silicon detector has to happen on a rather short time scale. However, we can build on our experience gained during the construction of the Run IIa silicon detector [5] and simpler fabrication and assembly methods should result in a much more efficient construction and testing cycle.

The inner two layers have a 12-fold crenellated geometry and will be mounted on a separate carbon fibre lined, carbon foam support structure. Figure 9.2 shows a drawing of the innermost layer. Due to the lack of space and severe cooling requirements, this layer has off-board electronics. The analog signals are transmitted through up to 420 mm long cables, wire-bonded to the silicon sensors, to a hybrid where the signals will be digitised and sent to the data acquisition system. Keeping the hybrid mass out of the detector active area region helps in reducing photon conversions. The design and operation of a long low-mass analog cable with very fine pitch is non-trivial concerning pick up noise and fabrication issues [6]. In collaboration with the Swiss company Dyconex [7] we have started to develop several cable prototypes based on different design layouts.

References

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